5-6 GHz SiGe VCO With Tunable Polyphase Output for Analog Image Rejection and I/Q Mismatch Compensation

David I. Sanderson and Sanjay Raman

Wireless Microsystems Laboratory, Bradley Dept. of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061

Abstract — **Image rejection and demodulation quality are adversely affected by in-phase and quadrature (I/Q) channel phase mismatch. This paper presents a 5-6 GHz Silicon Germanium (SiGe) voltage controlled oscillator (VCO) and integrated polyphase filter with I/Q phase imbalance compensation. The design of the VCO is discussed, including considerations for high inductor quality factor (Q) and low VCO phase noise. From a 2.5 V supply, the VCO core consumes 3 mA. The simulated phase noise at 1 MHz from the carrier is –114.6 dBc/Hz. The I/Q imbalance of the polyphase splitter is tunable by means of series output varactors. The polyphase network design can compensate for ±4º I/Q phase imbalance, which could provide approximately 15 dB improvement in image rejection in a Weaver architecture receiver.**

I. Introduction

Many modern transceiver architectures require in-phase *and* quadrature (I/Q) signal generation for image rejection or vector modulation and demodulation. For example, the IEEE 802.11a standard for wireless local area networks (WLANs) in the 5-6 GHz U-NII band, requires I/Q phase generation for orthogonal-frequency division multiplexing (OFDM) modulation. The I/Q phase error of the local oscillator (LO) source directly affects the performance of the image cancellation and negative frequency rejection (NFR) of the demodulation [1].

Meanwhile, the Weaver architecture (Fig. 1) is widely employed for low-IF image rejection receivers [2]. Fig. 2 shows the improvement in image rejection that can be obtained by tuning to compensate for I/Q phase error. As the phase error of the IF mixer LO (ω_{LO2}) varies from 0º, the image rejection quickly deteriorates. However, if the RF mixer LO (ω_{LO1}) phase error is *tuned* to track the IF mixer LO phase error, the image rejection can be preserved. Image rejection remains within 3 dB of the minimum for I/Q phase errors up to 40º when such compensation is used. Without compensation, the image rejection varies by 3 dB for phase errors less than 1º.

Several methods of compensating for I/Q imbalance using baseband DSP have been demonstrated [3]. However, an analog approach is potentially desirable to reduce overall power consumption as well as DSP computation requirements.

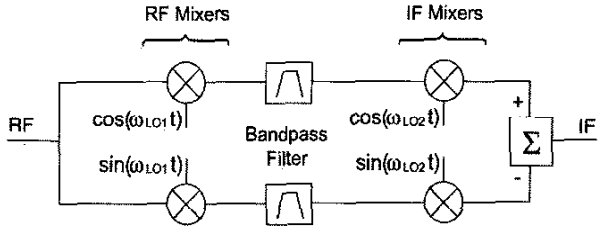

Fig. 1. Weaver image rejection architecture.

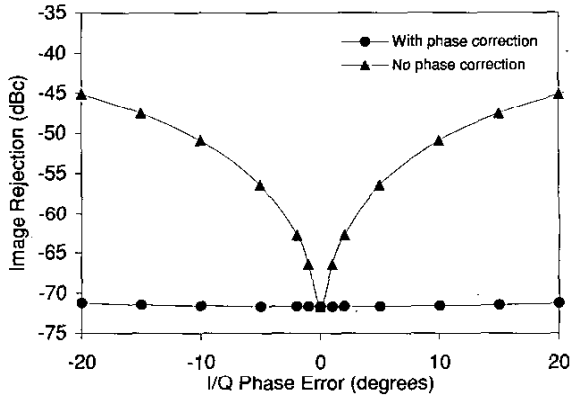

Fig. 2. Image rejection with and without phase correction from a system level simulation of a Weaver architecture receiver.

This paper presents a fully integrated, 5-6 GHz, *LC* voltage controlled oscillator (VCO) and tunable polyphase filter design. The tunable phase filter mitigates the effects of I/Q phase error on image rejection and demodulation.

II. Circuit Design

The technology used for this work is the Motorola 0.4 μm CDR1 SiGe BiCMOS process. This process has four metal interconnect layers and a thick-copper, last-metal layer for spiral inductors.

0-7803-7695-1/03/$17.00 © 2003 IEEE

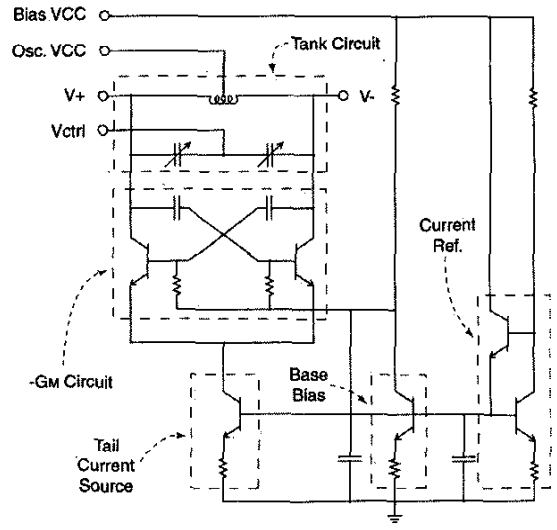

Fig. 3. Schematic of the unbuffered SiGe VCO.

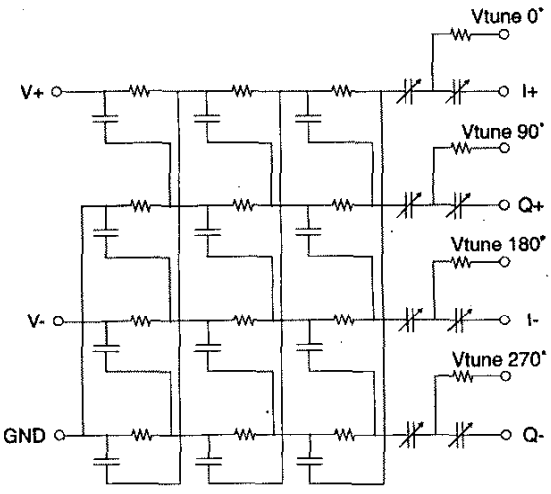

Fig. 4. Three pole *tunable* polyphase filter schematic.

A. Voltage Controlled Oscillator

Fig. 3 shows a schematic of the VCO circuit. The design is based on the well-known, cross-coupled, negative transconductance ($-G_M$) topology. SiGe heterojunction bipolar transistors (HBTs) were chosen for the $-G_M$ circuit for lower $1/f$ noise compared to MOSFETs. Furthermore, HBTs have a higher g_m/mA than MOSFETs, allowing for lower power consumption. The bases of the $-G_M$ HBTs are AC coupled to avoid saturation at high oscillation amplitudes (A_0) [4]. A current mirror and bias resistor set the base voltages. The varactors are accumulation mode devices available in the given technology.

Phase noise is inversely proportional to A_0. Therefore, the unbuffered oscillator was designed to have an A_0 of 1.5 V, which requires a high collector current through the $-G_M$ HBTs. The collector current in each device is set to 1.4 mA, to balance the trade-off between power consumption and A_0.

It is well known that increased tank circuit quality (Q) factor will improve VCO phase noise. A 3-port *symmetric* inductor was selected for this design; this structure has been shown to have Qs on the order of 50% higher than the equivalent dual inductor pair [5]. Sonnet em [6], a full-wave electromagnetic simulator, was used to predict the performance of the inductor during the design phase. At 5.25 GHz, the Q of the symmetric inductor was measured using on-wafer characterization techniques to be 15.4, versus 10.4 for an equivalent pair of inductors.

B. Polyphase Filter

Polyphase filters are extremely sensitive to variations in component values. Component mismatch and parasitic effects are the two main sources of I/Q phase error in the polyphase output [7]. Careful consideration to both of these effects is required in the circuit layout to obtain a low I/Q phase error. Components with relatively large physical area were selected to minimize mismatch. Layout symmetry aids in equalizing the parasitic resistance and capacitance of the routing paths.

Increasing the number of poles in the filter improves the bandwidth of the phase balance [8]. However, more poles introduce more loss, requiring more power consumption in the input and output buffers. A three-pole filter design was selected here to achieve reasonable phase flatness over the 675 MHz bandwidth of interest.

In traditional polyphase filters, adjusting the sizes of the series output capacitors after parasitic extraction of the layout minimizes the phase error. Inspecting the transfer function of these output capacitors reveals their effect on the output phase. For a given load impedance, R_L, the transfer function of the series output capacitor is:

$$G(j\omega) = \frac{j\omega R_L C}{1 + j\omega R_L C}. \quad (1)$$

The phase angle of the transfer function is:

$$\angle G(j\omega) = 90° - \tan^{-1}(\omega R_L C). \quad (2)$$

The transfer function of the polyphase filter is multiplied by (1) to give the overall transfer function. By changing C, the overall phase is adjusted. Thus, the capacitor values are typically adjusted during design such that the phase difference between each output is exactly 90º at the frequency of interest.

This work uses *tunable* capacitors in series with each output such that the phase can be actively tuned in the cir-

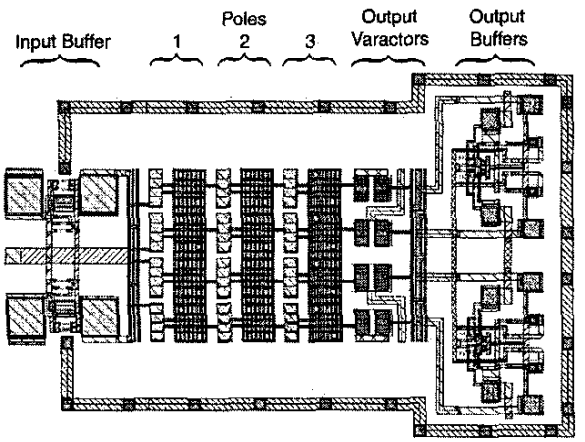

Fig. 5. Layout of the three-stage tunable polyphase filter. Die area is 276 μm x 161 μm.

cuit, post-fabrication (see Fig. 4). These tunable capacitors are also implemented with accumulation mode varactors. The resistors in series with the polyphase output control voltages prevent RF leakage through the DC supply path. The four polyphase output varactor control voltages can be tuned independently to adjust the overall I/Q phase error and the individual I or Q channel differential phase errors. In addition, tuning all the varactors together to the same value changes the frequency at which the phase error is zero (ideally). Alternatively, the varactor control voltages can be adjusted dynamically to compensate for I/Q imbalance in other parts of the RF system and at different frequencies.

C. Input and Output Buffers

The input buffer for the polyphase filter is the VCO output buffer. This buffer provides a high output impedance to the VCO. A class-AB, CMOS buffer is used because of its relatively high compression point for the large signal output of the VCO. Alternatively, a capacitive divider could be employed to reduce the VCO output swing into the buffer.

The output buffer is a differential pair amplifier designed to offset the 18 dB of loss through the polyphase splitter. There are two output buffers: one for the differential I outputs and a second for the differential Q outputs.

III. Layout and Fabrication

Fig. 5 shows the layout of the tunable polyphase filter. The differential RF input is on the left side of the figure and the differential I/Q output is on the right. The four large blocks to the right of the filter poles are the tunable output capacitors. All traces between the three stages are laid out in a grid to equalize the parasitics of each phase path.

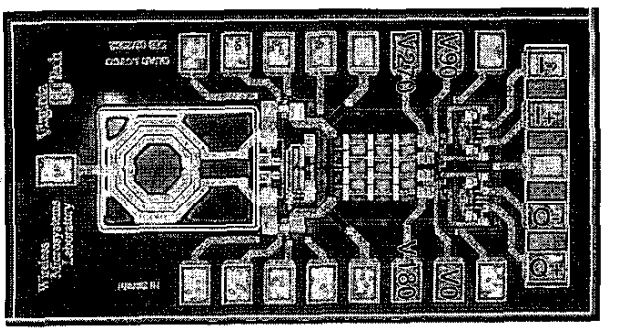

Fig. 6. Die photo of SiGe VCO and polyphase splitter fabricated in the Motorola CDR1 process. Die area is 1.5 mm x 0.76 mm.

Fig. 6 shows a die photo of the VCO and integrated tunable polyphase splitter. The quadrature outputs are located on the left side of the chip. The VCO and polyphase filter are laid out to equalize the parasitics and routing lengths for both the I and Q channels.

Several precautions were taken to minimize substrate noise coupling during layout. A ring of grounded substrate ties surrounds the polyphase splitter and provides isolation from the buffers and VCO circuit. In addition, the VCO symmetric inductor is separated from the active circuits by at least 100 μm to minimize magnetic coupling away from the coils. RF pads, with a reversed biased *p-n* junction lying under the pad metal, are used for the RF quadrature outputs. The *p-n* junction provides excellent isolation from substrate noise.

For testing, the chip is to be packaged in a low profile, 24 pin, 4 mm x 4 mm package. The relative length of the bond wires could have a significant effect on the output phase imbalance. Thus, the output bond pads are placed so that the bond wires will be the same length for each of the four outputs of the polyphase splitter.

IV. Simulated Results

The unbuffered VCO consumes 3 mA of current from a 2.5 V DC supply and has a peak output voltage of 1.0 V. The VCO and polyphase splitter combination consumes 24.5 mA from a 2.5 V source. Approximately 65% of the total current consumed is attributable to the VCO output buffer. Low power improvements in the VCO buffer would clearly achieve the largest improvements in overall circuit power consumption. In any event, power consumption is an acceptable tradeoff for an analog solution in light of the potential for lower computation power required in the baseband DSP.

The VCO tunes from 5.03 GHz to 5.90 GHz for tank varactor control voltages from 2.5 V to 0.5 V (see Fig. 7). All three of the 100 MHz U-NII bands from 5.15 to 5.825 GHz are covered by the VCO, making it useful for direct

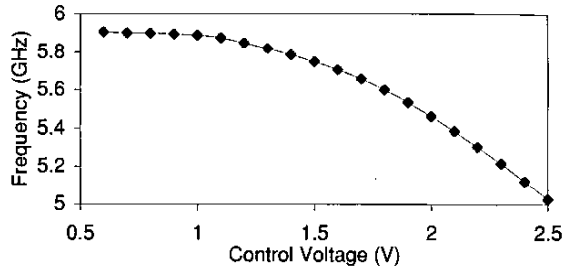

Fig. 7. Frequency of oscillation vs. control voltage.

conversion or low-IF receiver applications in this frequency space.

Simulations predict a phase noise of −114.6 dBc/Hz at a 1 MHz offset from the carrier. This exceeds the −107 dBc/Hz specification for the 802.11a standard [9].

A plot of the tunable polyphase I/Q phase imbalance is shown in Fig. 8. Simulated results are shown for polyphase output varactor control voltages from 0 to 1.25 V. Beyond 1.25 V, the phase does not change substantially. If all four varactor control voltages are set to zero, the I/Q phase error is zero (i.e., 90° phase balance). As the Q+ and Q- polyphase output varactor control voltages are increased together from zero volts while holding the I+ and I- control voltages at zero, the I/Q phase error increases to a maximum of 4°. If the I channel control voltages are increased while holding the Q channel control voltages constant, the same imbalance is attained, except that the phase error decreases toward a negative imbalance. This bi-directional tunability allows the polyphase to compensate for any phase error within ±4°.

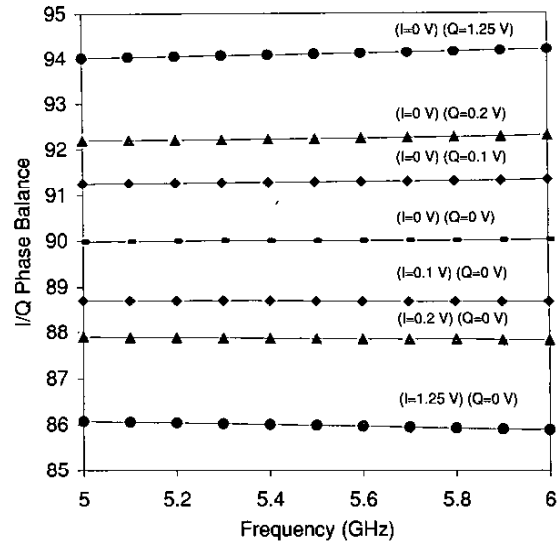

Fig. 8. Plot of tunable I/Q phase imbalance vs. frequency for various polyphase output varactor control voltages.

V. Conclusion

A 5-6 GHz *LC* VCO with an integrated tunable polyphase filter has been presented. To the authors' knowledge, this is the first phase-tunable polyphase network presented in the literature. Moreover, the resulting quadrature output VCO has a smaller die area than coupled-VCO topologies previously published. Potential applications include analog image rejection and I/Q phase error compensation.

Due to complications encountered with the packaging, measurements have not yet been completed. Measured performance for the VCO with and without polyphase outputs will be presented at the symposium.

Acknowledgement

This work was supported by a 2000 National Science Foundation (NSF) PECASE award. The authors wish to thank Motorola, Inc., Semiconductor Products Sector (SPS) for providing access to their 0.4 μm CDR1 SiGe BiCMOS process, specifically Eric Maass, Karen Dotson, and Brian Kump for assistance with CAD and fabrication issues.

References

[1] B. Côme, R. Ness, *et. al.*, "Impact of front-end non-idealities on Bit Error Rate performance of WLAN-OFDM transceivers," in *2000 RAWCON*, Sept. 2000, pp. 91-94.

[2] T.H. Lee, H. Samavati, and H.R. Rategh, "5-GHz CMOS wireless LANs," *IEEE Trans. on MTT*, vol. 50, no. 1, pp. 268-280, Jan. 2002.

[3] E. Cetin, I. Kale, and R.C.S. Morling, "On the performance of a blind source separation based I/Q corrector," in *2002 RAWCON*, Sept. 2002, pp. 99-102.

[4] C. Samori, S. Levantino, and A.L. Lacaita, "Integrated *LC* oscillators for frequency synthesis in wireless applications," *IEEE Comm. Mag.*, vol. 40, no. 5, pp. 166-171, May 2002.

[5] M. Danesh and J.R. Long, "Differentially Driven Symmetric Microstrip Inductors," *IEEE Trans. on MTT*, vol. 50, no. 1, pp. 332-340, Jan. 2002.

[6] Sonnet Software, Inc., 2002, *Sonnet em Suite, Release 8.52.001 Beta*, Liverpool, NY: Sonnet Software, Inc.

[7] F. Behbahani, Y. Kishigami, J. Leete, and A.A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE JSSC*, vol. 36, no. 6, pp. 873-886, June 2001.

[8] S.H. Galal, H.F. Ragaie, and M.S. Tawfik, "*RC* sequence asymmetric polyphase networks for RF integrated transceivers," *IEEE TCAS II*, vol. 47, no. 1, pp. 18-27, Jan. 2000.

[9] J. Bhattacharjee, D. Mukherjee, *et. al.*, "A 5.8 GHz fully integrated low power low phase noise CMOS *LC* VCO for WLAN applications," in 2002 *IEEE RFIC*, June 2002, pp. 475-478.